

Appl. No. 10/808,802
Amdt. dated 11/1/04
Reply to Office Action of 08/03/2004

Attorney Docket No.: N1085-90102
TSMC 2003-0186

Amendments to the Claims:

This listing of claims will replace all prior versions, and listing, of claims in the application:

1 1. (Amended) A method of forming an opening in a stack of insulator layers,
2 comprising the steps of:
3 providing a conductive structure;
4 forming said stack of insulator layer on said conductive structure, with said stack
5 of insulator layers comprised of an a first liner layer, an overlying first insulator layer, a
6 second liner layer, an overlying second insulator layer, an anti-reflective coating (ARC),
7 layer; and a capping, third insulator layer;
8 forming a via opening in a first portion of said stack of insulator layer, with said
9 via opening terminating in said first liner layer;
10 forming a photoresist shape including a trench-defining shape and a photoresist
11 plug that completely fills said via opening;
12 forming a trench opening in a second portion of said stack of insulator layers
13 using a said photoresist trench-defining shape as an etch mask, with said trench
14 opening terminating on top surface of said second liner layer, ~~and forming a photoresist~~
15 ~~plug in said via hole, located on said first liner layer;~~
16 removing portion of said second liner layer exposed in said trench opening;
17 removing said photoresist shape ~~and~~ including said photoresist plug; and
18 removing portion of said first liner layer exposed in said via opening, exposing a
19 portion of a top surface of said conductive structure.

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- 1 2. (Original) The method of claim 1, wherein said conductive structure is
2 comprise of copper.
- 1 3. (Original) The method of claim 1, wherein said first liner is a silicon nitride
2 layer, obtained via plasma enhanced chemical vapor deposition (PECVD) procedures at
3 a thickness between about 400 to 600 Angstroms.
- 1 4. (Original) The method of claim 1, wherein said first insulator layer is a
2 fluorinated silica glass (FSG) layer, obtained via PECVD procedures at a thickness
3 between about 500 to 1000 Angstroms.
- 1 5. (Original) The method of claim 1, wherein said second liner layer is a
2 silicon nitride layer, obtained via PECVD procedures at a thickness between about 200
3 to 400 Angstroms.
- 1 6. (Original) The method of claim 1, wherein said second insulator layer is a
2 silicon oxide layer, obtained via PECVD procedures at a thickness between about 500
3 to 1000 Angstroms.
- 1 7. (Original) The method of claim 1, wherein said ARC layer is a silicon
2 oxynitride layer, obtained via PECVD procedures to a thickness between about 500 to
3 700 Angstroms.
- 1 8. (Original) The method of claim 1, wherein said capping, third insulator
2 layer is a silicon oxide layer, obtained via PECVD procedures at a thickness between
3 about 500 to 700 Angstroms.
- 1 9. (Original) The method of claim 1, wherein said via opening is defined in
2 said capping, third insulator layer, in said ARC layer, in said second Insulator layer, in

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3 said second liner layer, and in said first insulator layer, via an anisotropic reactive ion
4 etching (RIE) procedure, using CHF_3 as an etchant for said capping, third insulator
5 layer, for said second insulator layer, for said ARC layer and for said first insulator layer,
6 while CH_xF_y or CF_4 is used as an etchant for said second liner layer.

1 10. (Original) The method of claim 1, wherein the diameter of said via
2 opening is between about 0.25 to 2.5 μm .

1 11. (Original) The method of claim 1, wherein said trench opening is defined
2 in said capping, third insulator layer, in said ARC layer, and in second insulator layer via
3 an anisotropic RIE procedure using CHF_3 as an etchant.

1 12. (Original) The method of claim 1, wherein portion of said second liner
2 layer exposed in said trench opening, is removed via a selective RIE procedure using
3 CF_4 or CH_xF_y as an etchant.

1 13. (Amended) The method of claim 1, wherein said photoresist shape ~~and~~
2 ~~said photoresist plug are~~ is removed using plasma oxygen ashing procedures.

1 14. (Original) The method of claim 1, wherein portion of said first liner layer
2 exposed in said via opening, is removed via a selective RIE procedure using CF_4 or
3 CH_xF_y as an etchant.

1 15. (Original) The method of claim 1, wherein the etch rate ratio of silicon
2 nitride of said first liner layer, to silicon oxide, during the selective RIE procedure used
3 to remove portion of said first liner layer exposed in said via opening, is between about
4 5 to 1, to 10 to 1 using CF_4 or CH_xF_y as an etchant.

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16. (Amended) A method of forming a dual damascene opening in a stack of insulator layers featuring a two step stop layer removal procedure, comprising the steps of:

providing a copper structure;

forming said stack of insulator layers on said copper structure, with said stack of insulator layers comprised of an underlying first silicon nitride stop layer, an overlying first dielectric layer, a second silicon nitride stop layer, a second dielectric layer, an anti-reflective coating (ARC) layer, and a capping silicon oxide layer;

forming a via opening in a first portion of said stack of insulator layer, with said via opening terminating in said first silicon nitride stop layer;

forming a photoresist shape including a trench-defining shape and a photoresist plug that completely fills said via opening and overlies a portion of a surface of said first silicon nitride layer;

forming a trench opening in a second portion of said stack of insulator layers using a said photoresist trench-defining shape as an etch mask, with said trench opening terminating on top said surface of said second silicon nitride stop layer, ~~and forming a photoresist plug in said via hole, overlying a portion of top surface of said first silicon nitride stop layer;~~

performing a first step of said two step stop layer removal procedure to selectively remove portion of said second silicon nitride stop layer exposed in said trench opening;

removing said photoresist shape ~~and~~ including said photoresist plug; and

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23 performing a second step of said two step stop layer removal procedure to
24 remove portion of said first silicon nitride stop layer exposed in said via opening,
25 exposing a portion of a top surface of said copper structure.

1 17. (Original) The method of claim 16, wherein said first silicon nitride stop
2 layer is obtained via plasma enhanced chemical vapor deposition (PECVD) procedures
3 at a thickness between about 400 to 600 Angstroms.

1 18. (Original) The method of claim 16, wherein said first dielectric layer is an
2 FSG layer, obtained via PECVD procedures at a thickness between about 500 to 1000
3 Angstroms.

1 19. (Original) The method of claim 16, wherein said second silicon nitride
2 stop layer is obtained via PECVD procedures at a thickness between about 200 to 400
3 Angstroms.

1 20. (Original) The method of claim 16, wherein said second dielectric layer is
2 a silicon oxide layer, obtained via PECVD procedures at a thickness between about 500
3 to 1000 Angstroms.

1 21. (Original) The method of claim 16, wherein said ARC layer is a silicon
2 oxynitride layer, obtained via PECVD procedures to a thickness between about 500 to
3 700 Angstroms.

1 22. (Original) The method of claim 16, wherein said capping, silicon oxide
2 layer is obtained via PECVD procedures at a thickness between about 500 to 700
3 Angstroms.

1 23. (Original) The method of claim 16, wherein said via opening is defined in
2 said capping silicon oxide layer, in said ARC layer, in said second dielectric layer, in

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3 said second silicon nitride stop layer, and in said first dielectric layer via an anisotropic
4 reactive ion etching (RIE) procedure, using CHF_3 as an etchant for said capping silicon
5 oxide layer, for said ARC layer and for said second dielectric layer and for said first
6 dielectric layer, while CF_4 or CH_xF_y is used as an etchant for said second silicon nitride
7 stop layer.

1 24. (Original) The method of claim 16, wherein the diameter of said via
2 opening is between about 0.25 to 2.5 μm .

1 25. (Original) The method of claim 16, wherein said trench opening is defined
2 in said capping silicon oxide layer, in said ARC layer, and in said second dielectric layer,
3 via an anisotropic RIE procedure using CHF_3 as an etchant.

1 26. (Original) The method of claim 16, wherein said first step of said two step
2 stop layer removal procedure, used to selectively remove portion of said second silicon
3 nitride stop layer exposed in said trench opening, is performed via a selective RIE
4 procedure using CF_4 or CH_xF_y as an etchant.

1 27. (Amended) The method of claim 16, wherein said photoresist shape ~~and~~
2 ~~said photoresist plug are~~ is removed using plasma oxygen ashing procedures.

1 28. (Original) The method of claim 16, wherein said second step of said two
2 step stop layer removal procedure, used to selectively remove portion of said first silicon
3 nitride stop layer exposed in said via opening, is performed via a selective RIE
4 procedure using CF_4 or CH_xF_y as an etchant.

1 29. (Original) The method of claim 16, wherein the etch ratio of silicon nitride
2 to silicon oxide, during said second step of said two step stop layer removal procedure
3 performed via a selective the selective RIE procedure used to remove portion of said

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- 4 first silicon nitride stop layer exposed in said via opening, is between about 5 to 1, to 10
- 5 to 1 using CF_4 or CH_xF_y as an etchant.